Advanced BIOS Settings

Auto Configuration:

- When enabled you won't be able to change advanced DRAM Timing options. If you want to get the most out of your system, you should **disable this setting**. Note: On some systems you can't disable the Auto Configuration.

DRAM Timing:

- **60ns**: specifies the DRAM read/write timing. 60ns will give you a higher system performance. Select this if you have EDO, 60ns FPM RAM or 70ns RAM.
- 70ns: Select this if your system crashes a lot with 60ns

L1 / L2 Cache Update Mode:

- Available options: WB (Writeback), WT (writethrough)
- **WB (Writeback)**: There are two concepts of cache-handling. The first is the write-back, you work against the cache, and when that data is finished, it's written back to the primary memory. You should put it as write-back to recieve the best performance.
- WT (Writethrough): The second one is the write-through, that instead of waiting until the work with the data is finished writes to the primary memory for every change in the cache.

L2 (WB) Tag Bit Length:

- This option is used to set secondary cache memory in write-back mode. When selecting the 7 bits it is running in write-back mode, and 8 bits, it is running in write-through mode.

  This option will not appear in all bioses/CMOSes as they may have the previous option of L1/L2 Cache Updat Mode. Also it is often represented as not only "7 bits", but rather 7+1 bits, and the alternative being 8+0 bits, as it will always work in the even amount of bits...i.e. Bytes!

  (Thanks to Leigh Green for giving me this info)

DRAM RAS# Precharge Time:

- This is an option which will not and for that matter should not be found any more in the more modern computers as it is all determeined by the CPU itself. The DRAM RAS# is a data line of the Memory, Row Access Strobe. In older computers, the 386's and early 486's by changing this option you could marginally change the time the computer took to do certain mathematic functions, but apart from that it is a worthless option, as with Pentium and new 486's and new memory it does not make one little bit of difference. If you do happen to find it in your bios, just keep it set at it's default, or try putting it low, but you may find you have problems, especially if you have more than one type of RAM in your system, i.e EDO at 50ns and FPM at 70ns...conflicts can arise, BEWARE.

  (Thanks to Leigh Green for giving me this info)

Turbo Read Leadoff (TRL):

- This option, when enabled, enables bypass of the first input register in the DRAM data pipeline, resulting in a 1 HCLK pull-in of all read leadoff timings. TRL can

only be set to enabled in a cacheless configuration.
NOTE It is illegal to enable this feature if ERRCMD[1:0] is not 00.
50/60 MHz allows both Speculative Leadoff and Turbo Read Leadoff to be enabled, whereas 66 MHz only allows Speculative Leadoff to be enabled.

(Thanks to Ray Van Tassle for giving me this info)

Fast RAS to CAS Delay:

- This is the amount of clock cycles it shall take for the Column Access Strobe to follow the Row Access Strobe. Set this as low as possible, but remember that not every RAM module is able to work with the lowest setting. Test your system afterwards !
  Note: RAS: ??? / CAS: ???
  This information comes from Tom's Hardware & Performance Guide

DRAM Read Burst (EDO/FP):

- Most accesses of the main memory are actually happening as a Burst. This is due to the cache not fetching only one DWord/Word/Byte, but rather than that fetching 4 or 8 consecutive DWords in a line. That's obviously much more effective than getting each byte on its own into the cache or the CPU. A burst read is done (in easy words) by telling the memory the first address first and then consecutive DWords can be read in a row, without telling the memory each address anymore. This obviously saves time. In clock cycles this looks then like x-y-y-y for a normal burst or x-y-y-y-z-y-y-y for a so called back-to-back burst. For Pipelined Burst Cache RAM e.g. this is 3-1-1-1 or 3-1-1-1-1-1-1-1. That's the amount of clock cycles the CPU needs for reading from its PB cache. Now for the main memory it's not a fixed value like for the PB cache, instead you can and have to adjust the x,y and sometimes also the z, due to the different DRAM types and speeds. Now after you've read this and hopefully understood it as well ;-), you see that the system will be faster when the x,y,z values are low rather than high, 'cause it takes the CPU less clock cycles to actually get the data it wants to process. The DRAM Read Timing is more or less the 'y'. Therefore you normally can choose from something like x222 and x333 for EDO (which is faster) and x333 and x444 for FPM RAM. You often have to choose it combined which each other, like x222/x333 and x333/x444, where the higher value stands for FPM, the lower for EDO RAM. **Choose the lowest possible value and try out your system !**
  This information comes from Tom's Hardware & Performance Guide

DRAM R/W Leadoff Timing:

- This one is the 'x' of the above described burst read/write. Here are some interesting differences between the Intel Triton FX and HX chipset. The FX can read fastest in a burst with 7-y-y-y, the HX is able to do 5-y-y-y - that's the reason why it's faster ! Writing in the FX is actually always done in a 5-y-y-y, the HX is also able to do a 4-y-y-y, but Intel recommends this only for 50 or 60 MHz bus clock. **And again keep it as low as possible. The value '5' for the HX chipset is mainly meant to only work well with 50ns or faster EDO.**
  This information comes from Tom's Hardware & Performance Guide

DRAM Write Burst Timing:

- Choose the lowest setting possible and test your system. (There is only one number here, e.g. x333 because the FPM and EDO Ram write accesses are the same).
  This information comes from Tom's Hardware & Performance Guide

Turbo Read Pipelining (Does anyone has info on this ?):

- **Enabled**: ????

Speculative Lead Off:

- **Enabled**: The 430HX chipset is capable of allowing a DRAM read request to be generated slightly before the address has been fully decoded. This can reduce read latencies. More simply, the CPU will issue a read request and included in this request is the place (address) in memory where the desired data is to be found. This request is received by the DRAM controller. When enabled, the controller will issue the read command slightly before it has finished determining the address.
  This information comes from Tom's Hardware & Performance Guide

Fast MA to RAS# Delay CLK:

- Available options: 1 CCLK, 2 CCLK
- Sets the delay between the end of a RAS cycle and the activation of the memory-addressbus (MA)

Fast EDO Path Select:

- When Enabled, a fast path is selected for CPU to DRAM read cycles for the leadoff. This results in a 1 HCLK pull-in for all read leadoff latencies for EDO DRAMS. This option should be set to Disabled if the EDO Read Burst timing is set to either x333 or x444. Disabled is the default.

Refresh RAS# Assertion:

- This option controls the number of clocks RAS# is asserted for refresh cycles. 5 CPU Clocks is the default.

ISA Bus Clock:

- By default the ISA Bus runs at 8.3 Mhz. Some motherboards have there ISA buses running conservatively at 7.15 Mhz. Some BIOS versions allow you to change the Mhz speed of the ISA Bus. I know that on an AMI BIOS, you usually have a set of choices such as "2/4 2/5 2/6 2/7 (etc)" or (1/2 1/3 1/4). It's a calculation: Motherboard clock speed * 2 (or 1), divided by the second digit. So on a 40Mhz motherboard, 2/6 becomes 40*2=80 divided by 6 = 13.3Mhz. Speeding up the ISA bus will have no effect no such things as sound cards, nor even on ISA IDE controllers (that't not the bottleneck on a PIO mode 0 drive). It's wonderful on ISA video cards though. Be careful, you can overclock. In my experience that will simply make the system unstable. Taking back down a notch will solve the problem.

  (Thanks to Christine Derksen for giving me this information)

System BIOS Cacheable:

- **Enabled**: Besides conventional memory, the system BIOS area is also cacheable.
- Disabled: Only conventional memory is cacheable.

Video BIOS Cacheable:

- **Enabled**: Besides conventional memory, the Video BIOS area is also cacheable.
- Disabled: Only conventional memory is cacheable.

8 Bit I/O Recovery Time & 16 Bit I/O Recovery Time:

- The 8/16 bit recovery time descripes how long apart (in sysclocks) two consecutive instructions will be issued to the I/O parts. You'll get faster performance when you lower this number. You should try out these settings and see what is best for you.

Peer Concurrency & Chipset NA# Asserted:

- **Enabled**: will accelerate operation speed of PCI bus, thus benefit to the system performance. But perhaps don't supper some expanded cards.
- Disabled: Only disable when Enabling these options give problems.
- Description: When PCE is enabled, the CPU will be allowed to run DRAM/L2 cycles when non-PHLD PCI masters are running non-locked cycles targeting PCI peer devices. CPU-to-PCI cycles will be blocked (BRDY# stalled) during these peer cycles. When PCE is disabled, the CPU will be held off the bus during PCI peer cycles. This should be set to enabled for normal operation.

    (Thanks to Ray Van Tassle for giving me this info)

Caching Options

To better understand these settings I'll give some definitions first:
- Write-back caching method: Write-back caching is the most effective caching method.
- Write-through caching method: Soon!
- TAG Ram: Soon!
- More...

1MB Cache memory:

- Available options: Disabled, Enabled
- ????

Alt Bit in Tag RAM:

- Available options: **7+1 Bits**, 8+0 Bits
- Tag bits are used to determine the state of the information that is stored in the L2 (external) cache. With this option the level of error determination is set. If you use the Write Back caching method use the 7+1 setting to receive best results.

Block-1 Memory Cacheable:

- Available options: No, **Yes**
- Choosing yes will cache the Local Memory Access Block-1

Burst Copy-Back Option:

- Available options: Disabled, Enabled
- Enabled: When a READ from the memory to the processor results in a cache miss, the chipset will try a second READ (in burst mode)

Burst SRAM Burst Cycle:

- Available options: 4-1-1-1, 3-1-1-1
- Lets you specify the timing of the burstmode Read and write cycles to and from the external cache memory (L2). Choose the lowest setting that works good.

Burst Write:

- Available options: Disabled, Enabled
- Enabled: The processor will write to the cache in burst mode.

CPU Cycle Cache Hit WS:

- Available options: Normal, Fast
- Normal: The cache-memory is refreshed by using normal processor cycles
- Fast: ???

CPU Write Back Cache:

- Available options: Disabled, Enabled
- Enabled: uses write back caching method. (for internal cache = L1 cache)
- Disabled: uses write through caching method.

C000 Cacheable:

- Available options: Disabled, Enabled

C000 Shadow Cacheable:

- Available options: Disabled, Enabled
- Same as above

Cacheable Range:

- Available options: 0-8M,...,0-128M
- Sets the memory area used for caching system-BIOSs or adapter-ROM BIOSs (e.g. SCSI BIOS)

Cache Burst Read:

- Available options: 1T, 2T
- Sets the needed time required to let the processor execute a cache-read operation in burst mode

Cache Burst Read Cycle:

- Available options: 1CCLK; 2 CCLK
- Sets the needed time required to let the processor execute a cache-read operation in burst mode

Cache Early Rising:

- Available options: Disabled, Enabled
- Enabled: The write-pulse rising edge method is used to write to the L2 cache (faster)
- Disabled: The normal write-pulse method is used.

Cache Read Timing / Cache Read Wait States:

- Available options: 0WS, 1WS
- Timing in wait-states for reading the L2 cache

Cache Tag Hit Wait States:

- Available options: 0WS, 1WS
- Timing in wait-states to test on a cache tag hit

Cache Timing Control:

- Available options: Fast, Medium, Normal, Turbo
- Sets the timing for reading from or writing to the cache-memory

Cache Update Policy:

- Available options: Write-back, write-through
- Sets the caching method for the L2 cache (external)

Cache Update Scheme:

- Available options: Write-back, write-through
- Sets the caching method for the L2 cache (external)

Cache Scheme:

- Available options: Write-back, write-through, W/B with dirty
- Sets the caching method for the L2 cache (external)
- W/B with dirty: The write-back caching method is used and dirty bits and tag bits are separated.

Cache Write Policy:

- Available options: Write-back, write-through
- Sets the caching method for the L2 cache (external)

Cache Write Cycle:

- Available options: 2T, 3T
- Timing in processor cycles for writing to the external cache.

Cache Write Timing:

- Available options: 0WS, 1WS
- Timing in wait-states for writing to the external cache.

Cache Write Wait States:

- Available options: 0WS, 1WS
- Timing in wait-states for writing to the external cache.

Combine Alter & Tag Bits:

- Available options: Combine, separate

Dirty pin selection:

- Available options: I/O, IN